Saturday, June 19, 10:20 a.m.
Chairpersons:     K. Nakamura, Analog Devices
                          S-H Lee, Sogang University

**25.1 ⎯ 10:20 a.m.**
**A 4 GS/s 6b Flash ADC in 0.13μm CMOS,** C. Paulus, H.-M. Blüthgen, M. Löw, E. Sicheneder, N. Brüels, A. Courtois, M. Tiebout and R. Thewes, Infineon Technologies, Munich, Germany

A 4GS/s 6b flash ADC with 8b output is presented realized in a 0.13μm standard CMOS technology. The outputs of 255 small-area comparators with comparatively large input offsets are averaged by a fault tolerant thermometer-to-binary converter. The ADC uses an on-chip low jitter VCO for clock provision and consumes 990mW at a single supply voltage of 1.5V. Dynamic measurements reveal proper operation up to input frequencies of 1GHz.

**25.2 ⎯ 10:45 a.m.**
**A 600-MSPS 8-bit Folding ADC in 0.18μm CMOS,** Z.-Y. Wang, H. Pan*, C.-M. Chang, H.-R. Yu and M.F. Chang, University of California, Los Angeles, CA, *Broadcom Corporation

An 8-bit folding A/D converter achieves SNDR of 40dB at 600MSPS for input signals up to 200MHz in standard 0.18um CMOS. Distributed T/Hs at the outputs of the first stage pre-amplifiers are employed instead of a dedicated front-end T/H. Lateral capacitors are inserted between adjacent T/H outputs to average the random mismatches in charge injection and clock skew among the distributed T/Hs. The ADC dissipates 207mW from a 1.8V supply.

**25.3 ⎯ 11:10 a.m.**
**A Highly Integrated Analog Baseband Transceiver Featuring a 12-bit 180MSPS Pipelined A/D Converter for Multi-Channel Wireless LAN,** K. Gulati, C. Muñoz, S. Cho, G. Manganaro, M. Lugin, M. Peng, A. Pulincherry, J. Li, A. Bugeja, A. Chandrakasan and D. Shoemaker, Engim, Inc., Acton, MA

**25.4 ⎯ 11:35 a.m.**
**A 1.5-V 10-b 50 MS/s Time-Interleaved Switched-Opamp Pipeline CMOS ADC with High Energy Efficiency,** B. Vaz, J. Goes and N. Paulino, UNINOVA-CRI, Monte da Caparica, Portugal

A 1.5V 10-b 50MS/s 2-channel pipeline ADC is described. Amplifiers are efficiently shared between channels using low-voltage techniques to reduce the power supply. The selected resolution per stage avoids the need of scaling the stages, simplifying the implementation of a low-power design. Measurements from the prototypes fabricated in a 0.18μm CMOS technology exhibit 10b DNL, 9.5b INL and 9.2 effective bits at Nyquist-rate. The chip occupies 1.3 mm2 and dissipates only 29 mW at 1.5V

**25.5 ⎯ 12:00 p.m.**
**0.9V 12mW 2MSPS Algorithmic ADC with 81dB SFDR,** J. Li, G.-C. Ahn, D.-Y. Chang and U.-K. Moon, Oregon State University, Corvallis, OR

An ultra low-voltage CMOS two-stage algorithm ADC incorporating background digital calibration is presented. The adopted low-voltage circuit technique achieves high-accuracy high-speed clocking without the use of clock boosting or bootstrapping. A resistor-based input sampling branch demonstrates high linearity and inherent low-voltage operation. The proposed background calibration accounts for capacitor mismatches and finite opamp gain error in the MDAC stages via a novel digital correlation scheme involving a two-channel ADC architecture. The prototype ADC, fabricated in a 0.18um CMOS process, achieves 81dB SFDR at 0.9V and 2MSPS (12MHz clock) after calibration. The ADC operates up to 5MSPS (30MHz clock) with 4dB degradation. The total power consumption is 12mW, and the active die area is 1.4~mm^2.